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EXAMINER	
KRASNIC, BERNARD	
ART UNIT	PAPER NUMBER
2624	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,922	PARK, HYUN-SANG	
	Examiner	Art Unit	
	BERNARD KRASNIC	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-48* is/are pending in the application.

4a) Of the above claim(s) *22-31,37-42 and 44-47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-18,20,21,32-35 and 48* is/are rejected.

7)☒ Claim(s) *19,36 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/14/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The amendment filed 1/24/2008 have been entered and made of record.

2. The Applicant has canceled claim(s) 2.

3. The application has pending claim(s) 1, 3-48, claims 22-31, 37-42 and 44-47 are withdrawn from consideration due to the Restriction Requirement dated 6/22/2007.

4. In response to the amendments filed on 1/24/2008:

The "Objections to the drawings" have been entered and therefore the Examiner withdraws the objections to the drawings.

The "Objections to the specification" have been entered and therefore the Examiner withdraws the objections to the specification.

The "Objections to the claims" have been entered and therefore the Examiner withdraws the objections to the claims.

The "Claim rejections under 35 U.S.C. 112, second paragraph" have been entered but the Applicant has not amended the addressed 35 U.S.C. 112 second paragraph issues and therefore the Examiner has once again addressed these issues.

The "Claim rejections under 35 U.S.C. 101" have been entered, and therefore the Examiner withdraws the 35 U.S.C. 101 rejections.

5. The Applicant's arguments with respect to claims 1, 3-21, 32-36, 43 and 48 have been considered but are moot in view of the new ground(s) of rejection because the Applicant has amended independent claim(s) 1 and 32 with the claim limitation "the encoder encoding the received image data" [this amendment was incorporated into the independent claims to overcome the 35 U.S.C. 101 rejections].

6. Applicant's arguments filed 1/24/2008 have been fully considered but they are not persuasive.

The Applicant alleges, "Rejections Under 35 U.S.C. 112 ..." in page 22, and states respectively that the term "substantially" is not vague or indefinite because it simply reflects and is intended to capture the variation in some additional range above or below the stated value. The Examiner disagrees and maintains the 35 U.S.C. 112 second paragraph rejections because the term "substantially" is vague and indefinite because this additional range is not defined and therefore could be understood differently dependent upon the interpreter.

The Applicant alleges, "Rengakuji is directed to an image processing ..." in pages 22-23 and "Applicant respectively submit that Rengakuji requires ..." in page 23, and state respectively that Rengakuji requires two pairs of writing address generators and reading address generators and generates separate read and write addresses which therefore fails to teach the generation of a common read/write address. The Examiner disagrees because Rengakuji discloses performing reading/writing of buffer memory 106 on the segments in units of MCU where the read out from / writing into buffer memory 106 in the order shown in Fig. 14 and as shown in Figs. 15A-15E [see

Rengakuji, col. 5, lines 63-67, col. 6, lines 1-2]. Rengakuji's Figs. 15A-15E are very similar to the Applicant's Figs. 7B-7D which illustrate a sequence of reading/writing segments in a line memory which just further shows that Rengakuji's reading/writing of buffer memory 106 is accomplished in the same manner as the Applicant's currently claimed invention.

In regards to the Applicant's amended limitation of "the encoder encoding the received image data", Rengakuji further discloses this claim limitation [see Rengakuji, Fig. 5, reference numbers 107-109].

Therefore claims 1, 3-21, 32-36, 43 and 48 are still not in condition for allowance because they are still not patentably distinguishable over the prior art reference.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 20-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re Claims 20 and 21, line 2 respectively: The limitation "to substantially equal" renders this claim indefinite and unclear because it is just a relative term. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 3-18, 32-35, and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Rengakuji (US 6,212,300 B1).

Re Claim 1: Rengakuji discloses an image processing apparatus for converting image data between a raster scan order and a block scan order (see col. 4, lines 41-45, abstract, the raster format is converted to a block format), comprising an image data processor (103-105) for supplying image data of a raster scan order having a given horizontal resolution and a given vertical resolution (see Fig. 5, col. 4, lines 34-61, any image has a HxV resolution, Figs. 6A-6B); a line memory (106) for storing image data of a plurality of lines / v=8 lines (see Fig. 5, col. 4,lines 41-45, v=8 lines); an address generating block (111-120, address generator) for converting supplied image data of raster scan order to block scan order (see col. 4, lines 41-45, abstract, the raster format is converted to a block format) by generating a common read/write address for the line memory so that only one line memory is required for read and write operations (see Fig. 5, col. 5, lines 5-28 and 41-48, the address to the free space created by reading out one MCU is a common read/write, performing reading/writing of buffer memory 106 on the

segments in units of MCU where the read out from / writing into buffer memory 106 in the order shown in Fig. 14 and as shown in Figs. 15A-15E [see Rengakuji, col. 5, lines 63-67, col. 6, lines 1-2]), the address generating block (111-120, address generator) including: a block address generator for generating an address of a block / segment which image data is read from and written into / read/write (see Fig. 14, col. 5, lines 63-66); a line offset generator for providing a line offset / first 8 lines 8H between an earlier common read/write address and a present common read/write address for the line memory (see col. 4, lines 41-45, col. 5, lines 52-67, col. 6, lines 1-2); and an address generator for generating the common read/write address for the line memory based on the block address / segments and the line offset / first 8 lines 8H (see Fig. 15A, see col. 4, lines 41-45, col. 5, lines 52-67, col. 6, lines 1-8, the figure shows the address generator creating the cell addresses (0) to (95) which are based on the 96 needed segments for the first 8 lines or as the applicant states a "phase"); and an encoder (107-109) receiving image data of the block scan order from the line memory and encoding the received image data (see Fig. 5).

Re Claim 3: Rengakuji further discloses the encoder (107-109) is a Joint Photographic Experts Group (JPEG) engine / JPEG compression (see Fig. 5, col. 1, lines 15-17, a typical DCT compressor is JPEG).

Re Claim 4: Rengakuji further discloses wherein the block includes image data of horizontal-direction pixels and vertical-direction pixels (see Fig. 1, the figures shows that each block has vertical and horizontal pixels).

Re Claim 5: Rengakuji further discloses wherein the block address generator provides a block offset between a start address of a present block and a start address of a next block for the line memory (see Figs. 15A and 15B, the block offset in these figures is 1 because the address of each adjacent block is 1 apart).

Re Claim 6: Rengakuji further discloses the block offset is initially set to 1 (see Figs. 15A and 15B, the block offset in these figures is 1 because the address of each adjacent block is 1 apart).

Re Claim 13: Rengakuji further discloses wherein the block address generator increases the block address as much as the block offset after the block address generator generates the common read/write addresses for a block (see Figs. 15A and 15B, the block offset in these figures is 1 because the address of each adjacent block is 1 apart).

Re Claim 15: Rengakuji further discloses wherein the block offset is set to the line offset at an end of every phase (the block offset in Fig. 15B is initially 1 because the address of each adjacent block is 1 apart but then changes to 8 [8 represents the line offset, 8

lines] as seen in Fig. 15C where the address of each adjacent block is 8 apart, looking at Figures 15B-15E [four of the applicants phases] and looking at Figs. 7B-7E of the Applicants Drawings it is seen that this block offset is correspondent between the two).

Re Claim 18: Rengakuji further discloses wherein image data having the given horizontal resolution (H) and the vertical resolution (V) comprises V/v phases, wherein v represents a number of vertical-direction pixels in a given block (see Fig. 1 and Figs. 15B-15E, there are four phases for the given horizontal and vertical resolution of the image wherein each table is representing a phase similarly to Figs. 7B-7E of the Applicants Drawings).

Re Claim 7: Rengakuji further discloses the line offset is initially set to a value defined by the given horizontal resolution divided by a number of horizontal-direction pixels in a given block (see col. 5, lines 63-68, col. 6, lines 2-8).

Re Claim 8: Rengakuji further discloses the line offset generator generates a next line offset / following 8 lines 8H between a present common read/write address and a next common read/write address for the line memory (see col. 4, lines 41-45, col. 5, lines 52-67, col. 6, lines 1-2, Figs. 15B-15E, a constant 8 line offset is followed going through the different four phases).

Re Claim 9: Rengakuji further discloses the block address and the next line offset are respectively reset at a start of every phase (see Figs. 15B-15E, it is seen that the block address is reset to 0 in the top left portion of each of the four phase tables and it is seen that the following / next line offset is reset to the 8 lines for the following phases).

Re Claim 16: Rengakuji further discloses the line offset is set to the next line offset at an end of every phase (see Figs. 15B-15E, the following / next line offset is reset to the 8 lines for the following phases).

Re Claim 17: Rengakuji further discloses a phase comprises an number of blocks equal to the given horizontal resolution divided by a number of horizontal-direction pixels in a given block (see Figs. 1 and 15B, col. 5, lines 52-67, col. 6, lines 1-8, it is seen that phase 1 in Fig. 15B has 96 segments or blocks which is relatively the same to the Applicants disclosure in paragraph [0050] of 80 segments or blocks).

Re Claim 10: Rengakuji further discloses the address generator generates an anchor address for the line memory based on the block address, and generates a sequential number of the common read/write address from the generated anchor address (see Figs. 14 and 15A, the anchor addresses are calculated, Figs. 15B-15E, col. 5, lines 63-67, col. 6, lines 1-30).

Re Claim 11: Rengakuji further discloses the address generator increases the anchor address to equal the line offset after the address generator generates the sequential number of the common read/write address (see Figs. 15A-15E, it is seen that the anchor address is increased from left to right and as the phase goes by it equals the line offset of 8).

Re Claim 12: Rengakuji further discloses the address generator decreases the anchor address to the given horizontal resolution minus one (H-1) when the anchor address has increased so as to equal or exceed (H-1) (see Figs. 14 and 15A, 7H/8+[H/8-1]=>H-1).

Re Claim 14: Rengakuji further discloses the block address generator decreases the block address to the given horizontal resolution minus one (H-1) when the block address has increased so as to equal or exceed (H-1) (see Figs. 14 and 15B-15E, 7H/8+[H/8-1]=>H-1).

Re Claim 32: Rengakuji discloses a method for converting image data between a raster scan order and a block scan order (see col. 4, lines 41-45, abstract, the raster format is converted to a block format), comprising receiving (106) image data of a raster scan order having a given horizontal resolution and a given vertical resolution (see Fig. 5, col. 4, lines 34-61, any image has a HxV resolution, Figs. 6A-6B, the line buffer 106 receives the raster format generated by 103-105); generating (111-120, address

generator) a common read/write address for a line memory (106) of a plurality of lines / v=8 lines (see Fig. 5, col. 5, lines 5-28 and 41-48, the address to the free space created by reading out one MCU is a common read/write, performing reading/writing of buffer memory 106 on the segments in units of MCU where the read out from / writing into buffer memory 106 in the order shown in Fig. 14 and as shown in Figs. 15A-15E [see Rengakuji, col. 5, lines 63-67, col. 6, lines 1-2]); reading image data of a block scan order / reads out block format from the common read/write address of the line memory (see col. 4, lines 41-45); storing image data of the raster scan order / image data of 8 lines stored in the common read/write address of the line memory (see col. 4, lines 41-45); converting stored image data of raster scan order to the block scan order (see col. 4, lines 41-45, abstract, the raster format is converted to a block format); and transmitting image data of the block scan order / block form to an encoder (107-109), the encoder encoding the received image data (see Fig. 5, col. 4, lines 46-49).

As to claim 48, the claim is the corresponding apparatus claim to claim 32 respectively. The discussions are addressed with regard to claim 32.

Re Claim 33: Rengakuji further discloses generating the common read/write address is based in part on generating an anchor address, the anchor address representing a segment of pixels of image data that is read from and written to the line memory (see Figs. 14 and 15A, the anchor addresses are calculated, Figs. 15B-15E, col. 5, lines 63-67, col. 6, lines 1-30).

Re Claim 34: Rengakuji further discloses the anchor address is generated based on at least one of a block address of a block, of the block scan order, in which image data is read from and written to in the line memory, and a block offset between a start address of a present block and a start address of a next block for the line memory (see Figs. 14 and 15A, the anchor addresses are calculated with regards to the block address, Figs. 15B-15E, col. 5, lines 63-67, col. 6, lines 1-30).

Re Claim 35: Rengakuji further discloses the anchor address is set based only on the block address (see Figs. 14 and 15A, the anchor addresses are calculated with regards to the block address, Figs. 15B-15E, col. 5, lines 63-67, col. 6, lines 1-30.

Allowable Subject Matter

11. Claims 19 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20-21 are dependent upon claim 19 [claims 20-21 are rejected under 35 U.S.C. 112 second paragraph though].
Claim 43 is dependent upon claim 19.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard Krasnic whose telephone number is (571) 270-1357. The examiner can normally be reached on Mon-Thur 8:00am-4:00pm and every other Friday 8:00am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on (571) 272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bernard Krasnic
April 28, 2008
/Jingge Wu/
Supervisory Patent Examiner, Art Unit 2624